

AMENDMENTS IN THE SPECIFICATION

Please replace the paragraph at page 6, line 23 with the following:

Thus, instructions following an incomplete[[d]] barrier operation, such as [[a]] loads/stores and other instructions, which may utilize the returned data, are executed without throttling the processor by first determining if the barrier operation completes successfully. The processor thus continues processing instructions as if no speculation has occurred. The MS flag remains set in the LRQ while the processor continues executing instructions. The MS flag is reset only when the sync ack is received. Because the speculative issuance of loads/stores beyond a barrier instruction have correct dependencies in over 99% of the times in high frequency processors, the processor continues to operate smoothly with an efficiency gain of up to 100 processor cycles when operating with full speculation.